Amendments of the Claims:

A detailed listing of all claims in the application is presented below. This listing of claims will replace all prior versions, and listings, of claims in the application. All claims being currently amended are submitted with markings to indicate the changes that have been made relative to immediate prior version of the claims. The changes in any amended claim are being shown by strikethrough (for deleted matter) or underlined (for added matter).

1. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a conductive electrode inside or on a surface of the fiber; ~~and~~

wherein an image on the display is addressed using an erase address waveform ~~drive control system, wherein said erase address drive control system includes:~~ which:

~~means for~~ stores~~ing~~ a charge on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding electrodes, thereby turning said at least one subpixel OFF.

2. (Currently Amended) A plasma display device according to claim 1, further comprising a ramped voltage address ~~drive control system~~ waveform, wherein said ramped voltage address waveform:~~drive control system includes:~~

~~means for~~ turn~~sing~~ each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding electrodes, thereby turning said at least one subpixel OFF.

3. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a conductive electrode inside or on a surface of the fiber; ~~and~~

wherein an image on the display is addressed using a write address waveform~~drive control system wherein said write address drive control system includes:~~which:

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~sing~~ charge to at least one subpixel by applying a voltage to its corresponding electrodes, thereby turning said at least one subpixel ON.

4. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

a glass plate with patterned sustain electrodes; ~~and~~

wherein an image on the display is addressed using an erase address waveform~~drive control system, wherein said erase address drive control system includes:~~ which:

~~means for~~ store~~sing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

5. (Currently Amended) A plasma display device according to claim 4, further comprising a ramped voltage address waveform~~drive control system~~ wherein said ramped voltage address waveform~~drive control system includes~~:

~~means for~~ turn~~sing~~ each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

6. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

a glass plate with patterned sustain electrodes; ~~and~~

wherein an image on the display is addressed using a write address waveform~~drive control system wherein said write address drive control system includes:~~ which:

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~sing~~ charge to at least one subpixel by applying a voltage to its corresponding sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

7. (Currently Amended) A plasma display device comprising:

at least one first fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

at least one second fiber structure including at least one wire sustain electrode located near a surface of said first fiber; ~~and~~

wherein an image on the display is addressed using an erase address waveform which:~~drive control system, wherein said erase address drive control system includes:~~

~~means for~~ store~~sing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

8. (Currently Amended) A plasma display device according to claim 7, further comprising a ramped voltage address waveform ~~drive control system~~ wherein said ramped voltage address waveform~~drive control system includes~~:

~~means for~~ turn~~sing~~ each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

9. (Currently Amended) A plasma display device comprising:

at least one fiber structure including a pair of barrier ribs that define a plasma channel, at least one wire address electrode inside or on a surface of said fiber, and a phosphor layer coating on said surface of said plasma channel; and

at least one second fiber structure including at least one wire sustain electrode located near a surface of said first fiber; ~~and~~

wherein an image on the display is addressed using a write address waveform which:~~drive control system wherein said write address drive control system includes:~~

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ adds~~ing~~ charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

10. (Currently Amended) A surface discharge plasma display device, comprising:

a first glass plate comprising a plurality of sustain electrodes, a thin dielectric layer covering said sustain electrodes and an emissive film covering said dielectric layer;

a fiber array including a plurality of fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel; and

a second glass plate, wherein said fiber array is sandwiched between said first glass plate and said second glass plate; ~~and~~

said plasma display being hermetically sealed with a glass frit around a perimeter of the first and second glass plates and said wire address electrodes are brought out through said glass frit for direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms~~drive control system~~ are~~is~~ selected from the group consisting of:

a) an erase address waveform~~drive control system~~;

b) a write address waveform~~drive control system~~; and

c) a ramped voltage address waveform~~drive control system~~.

11. (Currently Amended) The surface discharge plasma display device of claim 10, wherein said erase address waveform~~drive control system includes~~:

~~means for~~ store~~sing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~sing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

12. (Currently Amended) The surface discharge plasma display device of claim 10, wherein said write address waveform~~drive control system includes~~:

~~means for~~ remove~~sing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~sing~~ charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

13. (Currently Amended) The surface discharge plasma display device of claim 10, wherein said ramped voltage address waveform~~drive control system includes~~:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or add a charge for write addressing

~~means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and~~

~~means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF~~.

14. (Currently Amended) A surface discharge plasma display device, comprising:

two glass plates sandwiched around first and second orthogonal arrays of fibers defining a structure of said display;

said first fiber array including a plurality of top fibers, each top fiber including at least one pair of wire sustain electrodes located near a surface of said top fiber, said surface being covered by an emissive film;

said second fiber array including a plurality of bottom fibers, each bottom fiber including a pair of barrier ribs that define a plasma channel, at least one wire address electrode located near a surface of said plasma channel, and a phosphor layer coating on said surface of said plasma channel; ~~and~~

said plasma display being hermetically sealed around a perimeter of the glass plates with a glass frit and said pair of wire sustain electrodes and said wire address electrode are brought out through said glass frit for direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms are~~drive control system is~~ selected from the group consisting of:

a) an erase address waveform~~drive control system~~;

b) a write address waveform~~drive control system~~; and

c) a ramped voltage address waveform~~drive control system.~~.

15. (Currently Amended) The surface discharge plasma display device of claim 14, wherein said erase address waveform~~drive control system includes~~:

~~means for~~ stores~~ing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively removes~~ing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

16. (Currently Amended) The surface discharge plasma display device of claim 14, wherein said write address waveform~~drive control system includes~~:

~~means for~~ removes~~ing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ adds~~ing~~ charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

17. (Currently Amended) The surface discharge plasma display device of claim 14, wherein said ramped voltage address waveform~~drive control system includes~~:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or add a charge for write addressing

~~means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and~~

~~means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF~~.

18. (Currently Amended) An electronic display comprising at least one fiber including at least one wire electrode wherein said wire electrode is brought out through a seal region for

direct connection to a drive control system that generates a plurality of voltage waveforms, which address an image on the display;

wherein said waveforms are~~drive control system is~~ selected from the group consisting of:

a) an erase address waveform~~drive control system~~;

b) a write address waveform~~drive control system~~; and

c) a ramped voltage address waveform~~drive control system.~~.

19. (Currently Amended) The surface discharge plasma display device of claim 18, wherein said erase address waveform~~drive control system includes~~:

~~means for~~ store~~s~~~~ing~~ a charge over said sustain electrodes on each subpixel to turn each subpixel ON; and

~~means for~~ selectively remove~~s~~~~ing~~ said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.

20. (Currently Amended) The surface discharge plasma display device of claim 18, wherein said write address waveform~~drive control system includes~~:

~~means for~~ remove~~s~~~~ing~~ a charge from each subpixel, thereby turning each subpixel OFF; and

~~means for~~ add~~s~~~~ing~~ charge to at least one subpixel by applying a voltage to its corresponding wire sustain electrodes and wire address electrode, thereby turning said at least one subpixel ON.

21. (Currently Amended) The surface discharge plasma display device of claim 18, wherein said ramped voltage address waveform~~drive control system includes~~:

uses a ramp voltage to set the initial charge state of all the subpixels in the display to either charged for erase addressing or uncharged for write addressing; and

addresses at least one subpixel by selectively applying a voltage to its corresponding wire sustain electrodes and wire address electrode, wherein said voltages remove said charge for erase addressing or adds a charge for write addressing

~~means for turning each subpixel ON by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and~~

~~means for selectively removing said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel OFF.~~

22. (New) A plasma display device of claim 3, further comprising a ramped voltage, wherein a ramped voltage address waveform:

turns each subpixel OFF by applying at least one voltage ramp to at least one pair of sustain electrodes to remove the charge from each subpixel; and

selectively adds said charge to at least one subpixel by applying a write pulse to its corresponding electrodes, thereby turning said at least one subpixel ON.

23. (New) A plasma display device according to claim 6, further comprising a ramped voltage, wherein a ramped voltage address waveform:

turns each subpixel OFF by applying at least one voltage ramp to at least one pair of sustain electrodes to remove the charge at each subpixel; and

selectively adds said charge to at least one subpixel by applying an write pulse to its corresponding wire address electrode, thereby turning said at least one subpixel ON.

24. (New) A plasma display device according to claim 9, further comprising a ramped voltage, wherein a ramped voltage address waveform:

turns each subpixel OFF by applying at least one voltage ramp to at least one pair of sustain electrodes to create a standardized charge at each subpixel; and

selectively removes said charge from at least one subpixel by applying an erase pulse to its corresponding wire address electrode, thereby turning said at least one subpixel ON.